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# High power digital direction finding antennas

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## CENTER FOR JOINT SERVICES ELECTRONIC WARFARE

### High Power Digital Direction Finding Antennas

by

Phillip E. Pace

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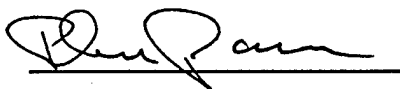
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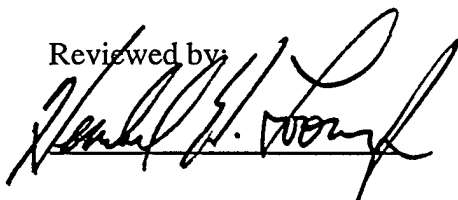
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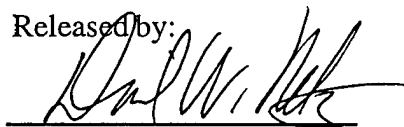
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13. ABSTRACT (Maximum 200 words)  A novel high-power digital direction finding antenna architecture is presented. Direct digitization of the antenna signal is accomplished using a symmetrical number system electro-optical wideband analog-to-digital converter. By directly digitizing the antenna signals, the need for down conversion and automatic gain control circuitry can be eliminated. The design of a 5-bit prototype that uses three integrated optical interferometers is discussed and its experimental DC performance (transfer function) is evaluated. The hardware realization of a three channel 14-bit device currently being constructed in the Optical Electronics Laboratory is also discussed.					
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# I Introduction

The task of a digital antenna is to accept electromagnetic (EM) voltages that represent physical emitters in the analog world and to convert those voltages to digital codes that can be stored or processed in digital computers. The direct conversion of these voltages at the antenna is performed by wideband high resolution analog-to-digital converters (ADCs). High performance ADCs are critical building blocks in a wide range of hardware, from radar and electronic warfare systems to multimedia based personal computers and workstations. The need constantly exists for converters with wide bandwidth, greater dynamic range, and lower power dissipation. A wider ADC bandwidth helps reduce the hardware needed to cover the EM spectrum of interest and can eliminate the need for down conversion to intermediate frequencies. A greater dynamic range removes the need for notch filters and automatic gain control circuits that can effectively hide important signals of interest.

ADCs that utilize integrated optical guided-wave technology play an important role in these types of systems. Using a parallel configuration of wideband interferometers to symmetrically fold the analog signal prior to quantization by high speed comparators (analog preprocessing), these high performance ADCs can directly digitize the EM signals from an antenna (digital antenna) [1-5]. Recently, a preprocessing approach was described that can be easily incorporated into the established techniques to provide an enhanced resolution capability using a minimal number of comparators loaded in parallel. The approach is based on preprocessing the analog signal with a symmetrical number system (SNS) [6-8]. The SNS preprocessing is used to decompose the analog amplitude analyzer operation into a number of sub-operations (moduli) that are of smaller computational complexity. Each sub-operation symmetrically folds the analog signal with folding period equal to the modulus. Thus, each

sub-operation only requires a precision in accordance with that modulus rather than the signal's entire dynamic range. A much higher resolution is achieved after the  $N$  different SNS moduli are used and the results of these low precision sub-operations are recombined. For example, using this scheme, a 10-bit three-channel ADC, can be formed using a total of 52 comparators with a maximum number of 15 comparators loaded in parallel.

Further refinement in the architecture of the SNS has led to an *optimum* scheme resulting in an even more efficient implementation [9–12]. For example, using the optimum SNS preprocessing, a 10-bit three-channel ADC can be formed using a total of 29 comparators with a maximum of 12 loaded in parallel. That is, by incorporating the optimum SNS encoding the number of comparators for any folding ADC is dramatically reduced.

This report details the advances made toward directly digitizing the signals from an antenna using electro-optics. In Section II, the design and performance of a 5-bit electro-optical SNS ADC that was constructed in the Optical Electronics Laboratory at the Naval Postgraduate School is described. In Section III the design and hardware construction of a 14-bit 5 MHz device is presented. System integration of this device is currently underway and will be tested in late September 1996. The significance of this work is that wideband, digitization of high power antenna signals can be accomplished more effectively using the optimum SNS encoding. By reducing the number of comparators that are required, the dynamic range of the converter can be efficiently increased without degrading the bandwidth capabilities. Using optical processors to fold the antenna signal and a high-speed laser for sampling, these high resolution SNS ADCs may be interfaced directly to a direction finding antenna eliminating the need for conventional down conversion and baseband processing [13].

## II Optimum 5-Bit SNS Electro-Optical ADC Architecture

The requirement for high speed, high resolution ADCs has led to the need for advanced technologies such as InP heterojunction bipolar transistors and resonant tunneling devices. However, the lack of a convenient high resolution encoding architecture inhibits the amount of progress that can ultimately be made. For example, GaAs comparators are currently available with bandwidths greater than 2 GHz. ADCs that use these devices, however, still require sample and holds which have bandwidths currently less than 1 GHz and suffer from an inefficient sampling process. Flash configurations have been demonstrated but are still limited to 4–7 bits. That is, the existing encoding methods have a very limited use in extending the resolution of these ADC architectures.

In an integrated optical guided-wave SNS ADC, three Mach-Zehnder interferometers are used to fold the analog waveform. The block diagram of a 5-bit three-channel SNS ADC is shown in Fig. 1. The RF analog signal to be digitized is applied in parallel to each interferometer and is sampled using a series of laser pulses. The important interferometer parameter to be considered is the maximum analog voltage  $V_{\max}$  that may be applied and still give a symmetrically folded waveform. Knowing  $V_{\max}$  the maximum number of folds available from the interferometer is

$$F = \frac{V_{\max}}{V_{\pi}} \quad (1)$$

where  $V_{\pi}$  is half the folding period. In the optimum SNS ADC, a complete fold is  $2m_i$  states. Therefore, the largest number of folds required in a  $B$  bit SNS ADC channel is

$$F_{\text{req}} = \frac{2^B - 1}{2m_{\min}} < \frac{V_{\max}}{V_{\pi}} \quad (2)$$

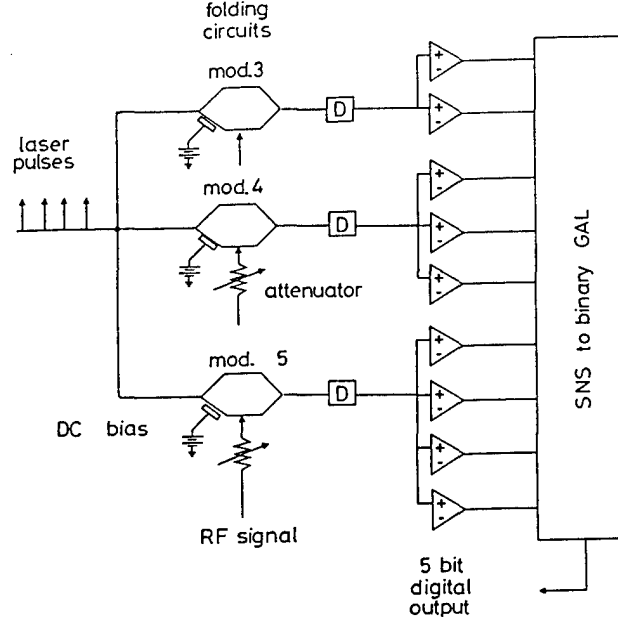


Figure 1: Schematic diagram of the 3 channel 5-bit integrated optical SNS ADC ( $m_1 = 3$ ,  $m_2 = 4$ ,  $m_3 = 5$ ).

where  $m_{\min}$  is the smallest modulus in the SNS system. The LSB code width is  $V_{\pi}/2m_i$ .

Each of the three identical LiNbO<sub>3</sub> interferometers were constructed by the Optical Sciences Division at the Naval Research Laboratory and were on-loan to the NPS Optical Electronics Laboratory for use in the 5-bit ADC ( $V_{\pi} = 2.25$  V). The  $V_{\max}$  was determined experimentally to be  $V_{\max} = 12$  V ( $\pm 12$  V). The number of symmetrical folds from (1) is 5.3. From (2), the minimum modulus is calculated to be  $m_{\min} = 3$ . The modulus for the resulting 5-bit system is then  $m_1 = 3$ ,  $m_2 = 4$ , and  $m_3 = 5$  with an LSB = 0.375 V. To provide the larger folding periods for the  $m_2 = 4$  and  $m_3 = 5$  channels, the analog signal is attenuated before being applied to each interferometer. To properly align (or phase) each channel, a small DC bias is applied to each interferometer. The properly folded and aligned waveforms are shown in Fig.



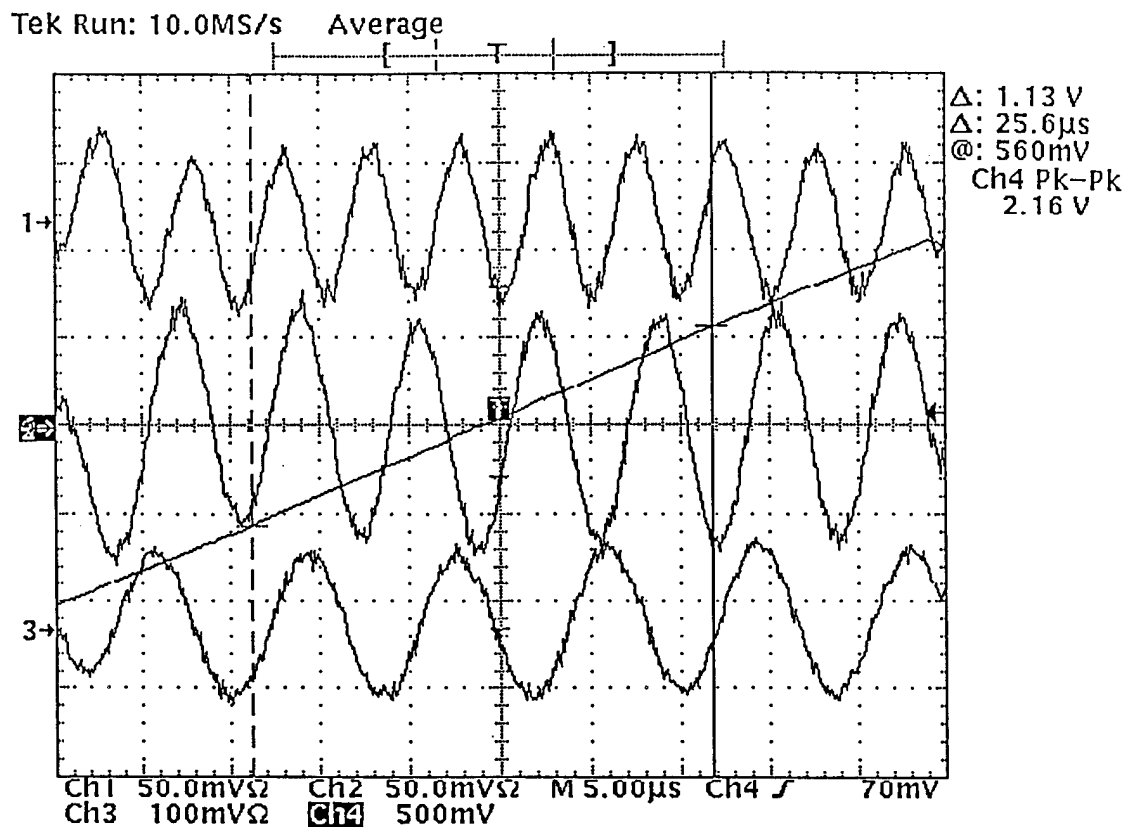


Figure 2: Interferometer symmetrical folding waveforms at detector output.

2. At the left edge of the ADC range, the folded waveforms are in nominal alignment. The 5-bit design requires a total of nine comparators (Analog Devices 9698). The SNS-to-decimal mapping function was instrumented using a single Lattice 22V10-15 generic array logic (GAL) device. The analog signal at the interferometers was sampled using a BCP-410 laser transmitter (sampling pulse width = 40 ns). To demonstrate the SNS ADC transfer characteristics, a 1 kHz triangular waveform was applied. The SNS ADC decimal output is shown in Fig. 3 [14]. Note the 32 distinct quantization levels. A 1 kHz sine waveform was also applied. Figure 4 shows the corresponding transfer characteristic for this input. These results serve to demonstrate the feasibility of the optical SNS ADC concept. As shown in Figs. 3 and

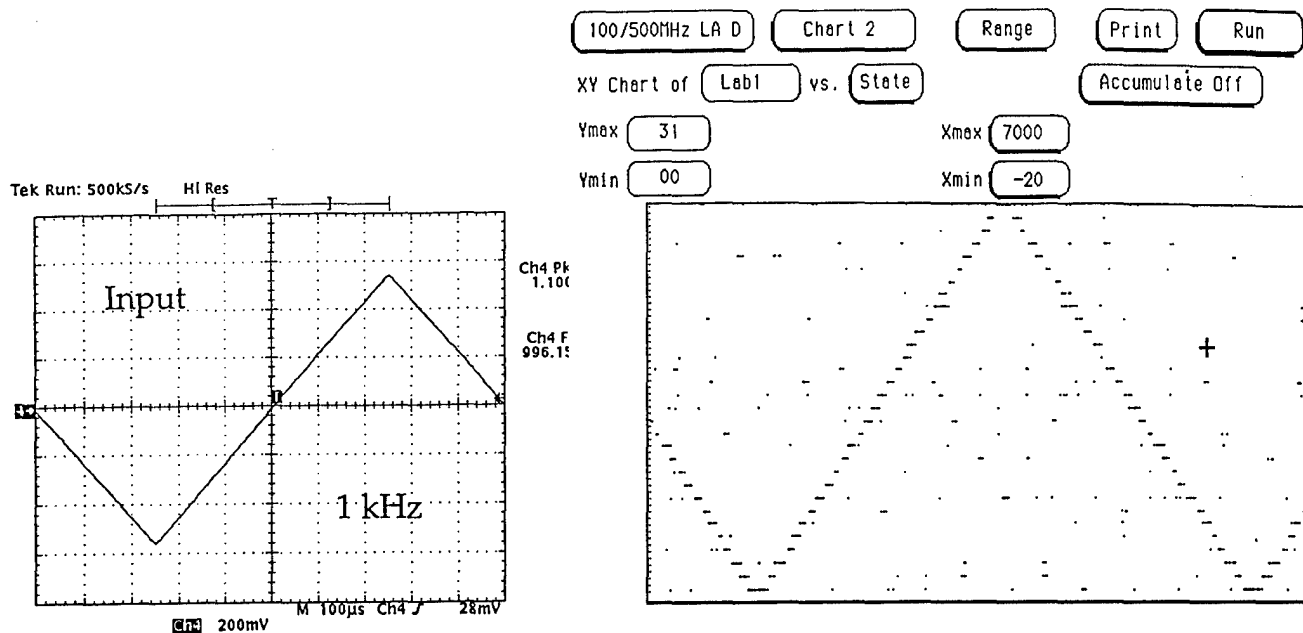


Figure 3: a) Triangular (1 kHz) input signal and b) SNS ADC output showing the 32 distinct levels.

4, a small amount of noise is present in the ADC output. This noise is due to encoding errors (glitches) that result when an input voltage lies at a code transition point. To eliminate these encoding errors, a few additional comparators in the smallest channel may be used. By computing the parity of the minimum modulus computer states, small bands may be set up about these transition points and the possible errors easily isolated and interpolation performed. This approach is currently being investigated for a 14-bit system, the results of which will be reported at a later date.

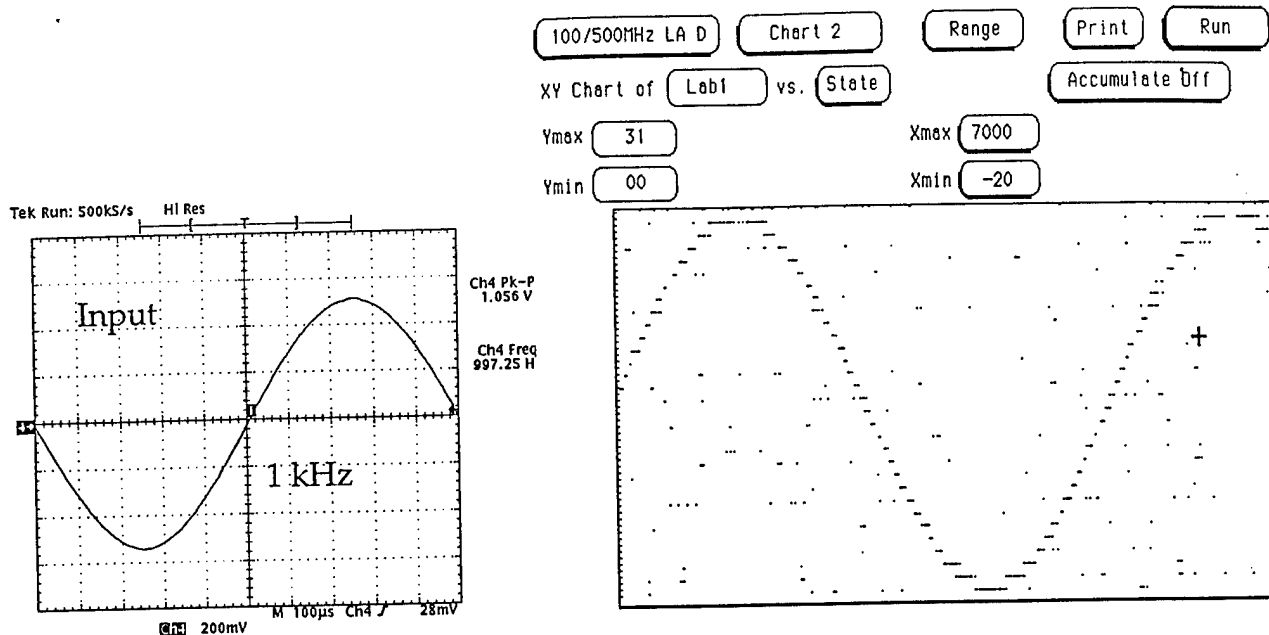


Figure 4: a) Sinusoidal (1 kHz) output signal and b) SNS ADC output showing the 32 distinct levels.

### III Optimum SNS 14-Bit 5 MHz Device

A block diagram of the 14-bit 3-channel electro-optical ADC is shown in Fig. 5. Each channel is configured for a different modulus ( $m_1 = 63$ ,  $m_2 = 64$ ,  $m_3 = 65$ ). A passive termination network with a front-end low-pass anti-aliasing filter is used within each channel to properly attenuate the antenna signal in the stop band  $f_s/2 = 2.5$  MHz. Three *reflective* Mach-Zehnder interferometers are used each with its own circulator to fold the input signal from the passive termination network. A pulsed laser source is used to sample the folded input signal and also drive the system clock. The detected output in each channel is then passed through a DC coupled wideband amplifier before being amplitude analyzed by the individual comparator arrays. Each array contains sixty-four comparators and a binary encoder are contained within a GaAs pin grid array (PGA). The four PGAs each encode the signal in a thermometer code format.

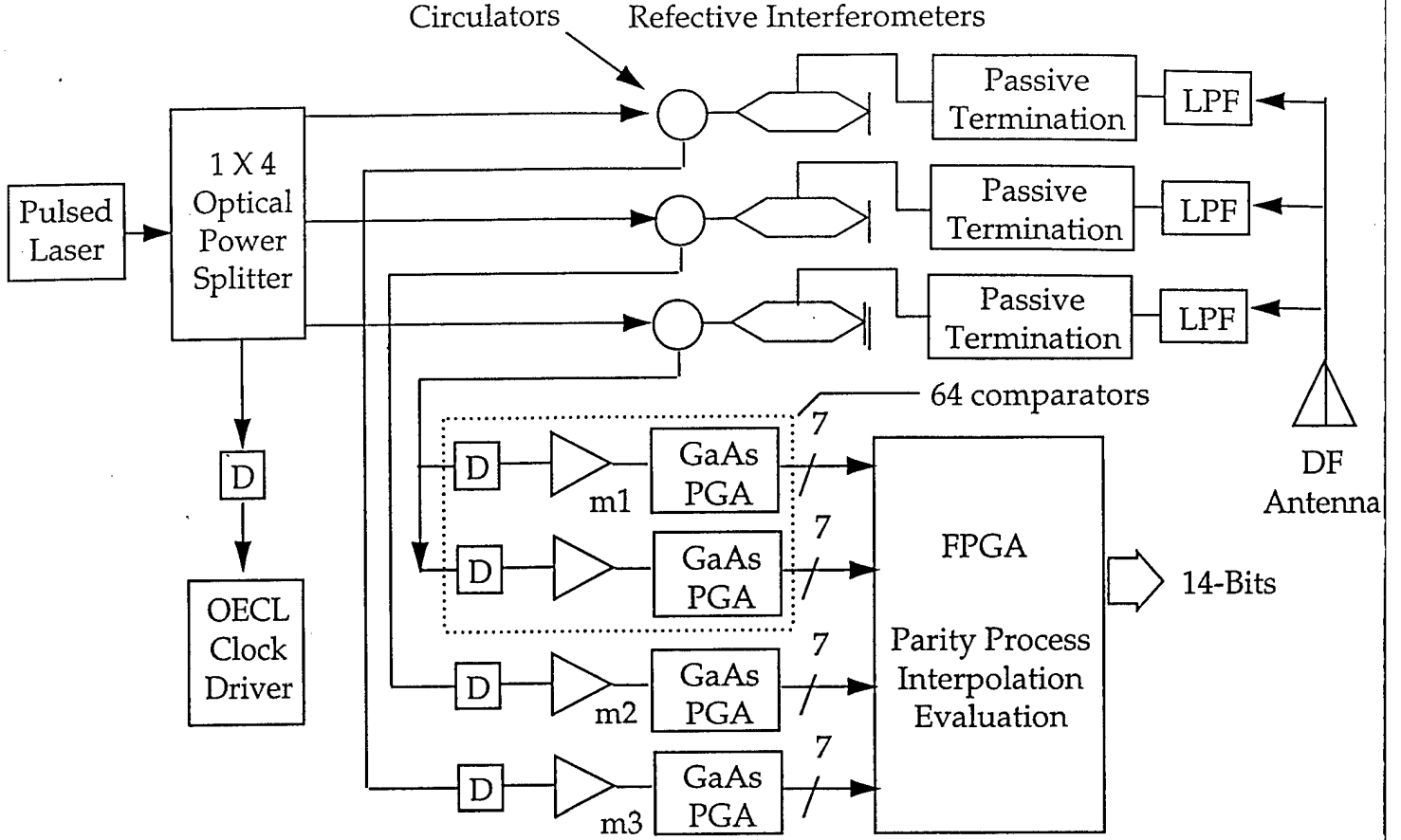
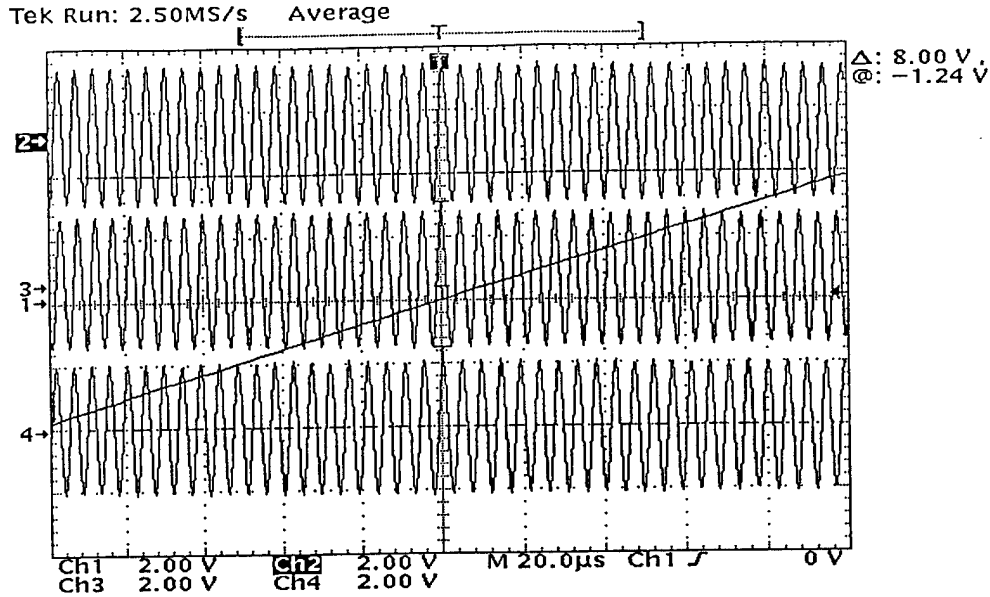


Figure 5: Schematic diagram of the 14-bit 5 MHz SNS ADC.

The thermometer code is then translated by the encoder into a 7-bit representation. Note for the  $m_1$  channel, two GaAs PGAs are used due to the parity and interpolation processing in the minimum modulus channel ( $2m_1 = 126$  comparators required). The parity and interpolation processing to output the correct 14-bit word is implemented in a field programmable gate array (FPGA).

The reflective interferometers give considerably better performance than those used for the 5-bit design and can efficiently couple the wideband signals into the optical domain. The  $V_\pi$  of each interferometer is  $V_\pi \cong 0.33$  volts. Figure 6 shows the transfer function for each device for a ramped signal from  $-14.8$  to  $14.8$  volts



$$V_{\pi} = 0.33 \text{ volts}$$

$$\text{Ramped Signal: } \pm 3.7 \times 4 = \pm 14.8 \text{ volts}$$

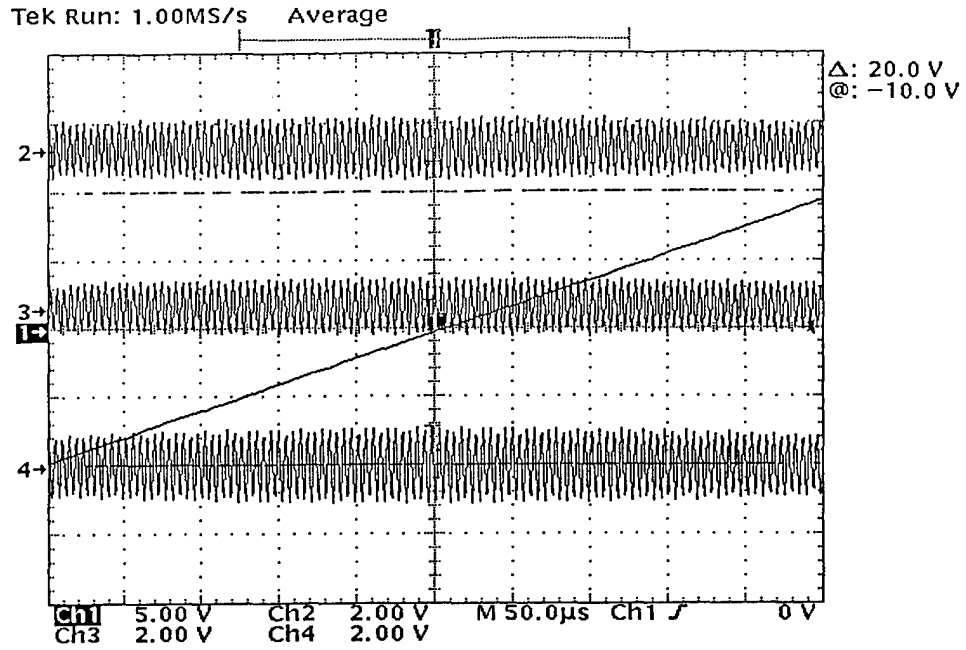
$$\# \text{Folds} = 45$$

Figure 6: Reflective interferometer symmetrical folding waveforms for the 14-bit SNS ADC ( $N_f = 45$ ).

(45 folds). Note the uniformity of the folded output waveforms. Figure 7 shows the transfer function for a ramped signal from  $-37$  volts to  $37$  volts (112 folds). The number of folds were counted individually for each of these devices with the results summarized in Table 1.

The schematic diagram for the termination network is shown in Fig. 8 [15]. Note that the network instruments the capability to passively change the folding period of the  $m_2$  and  $m_3$  channels. Also, the capability to add a small DC bias on each channel is included which is necessary to properly phase (or align) the folding waveforms.

The GaAs PGAs were designed by the Systems, Processes and Engineering Corporation (SPEC) and fabricated through MOSIS in Vitesse Semiconductors, H-GaAs



$$V_{\pi} = 0.33 \text{ volts}$$

$$\text{Ramped Signal: } \pm 3.7 \times 10 = \pm 37.0 \text{ volts}$$

$$\# \text{Folds} = 112$$

Figure 7: Reflective interferometer symmetrical folding waveforms for the 14-bit SNS ADC ( $N_f = 112$ ).

Table 1:

UTP Interferometer Number	Number of Folds ( $V_{pp} = 39.237 \text{ V}$ )	Number of Folds ( $V_{pp} = 86.0 \text{ V}$ )
1142	57.8	126.8
1143	57.6	126.2
1144	58.0	127.1

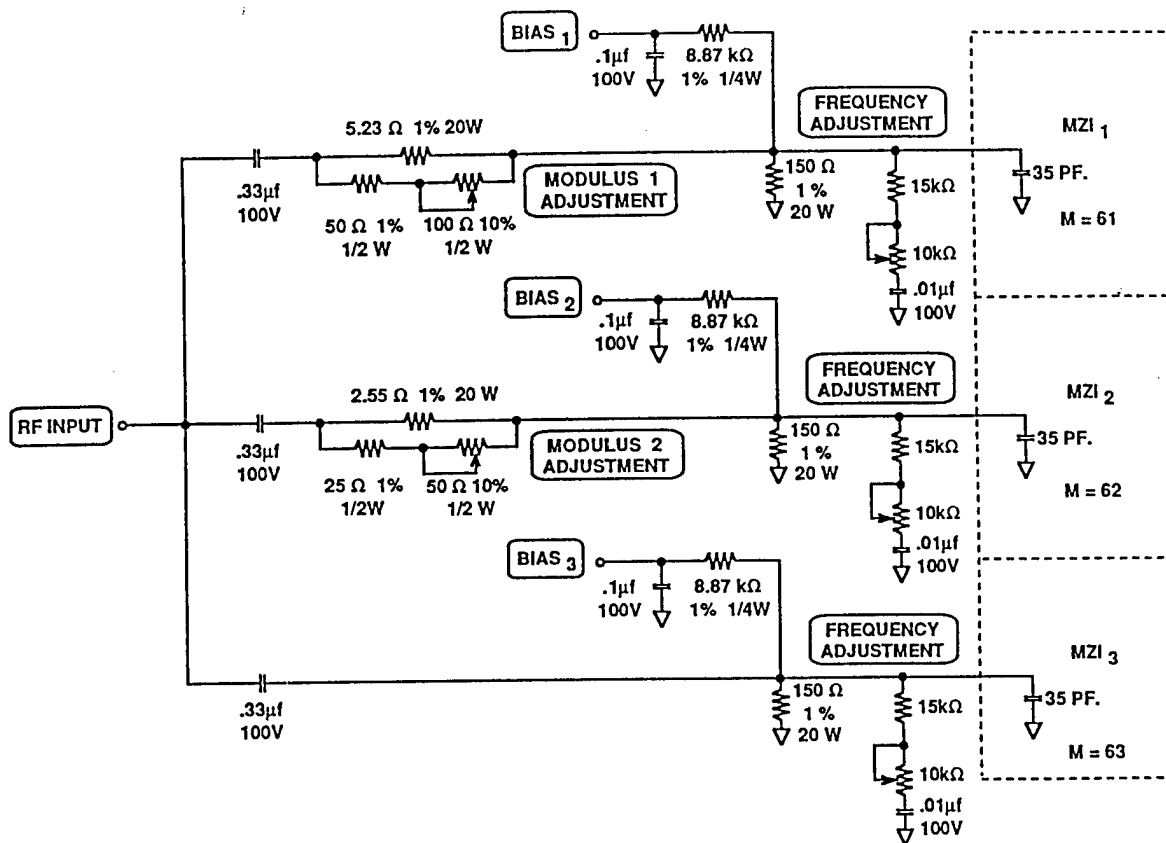


Figure 8: Termination network and interface to the interferometer folding circuits.

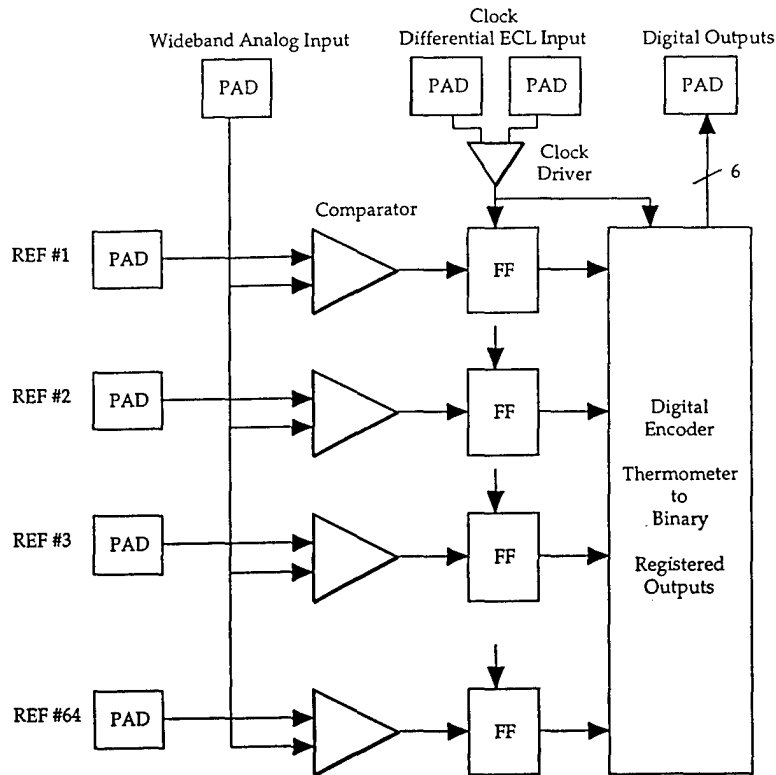


Figure 9: Block diagram of the GaAs integrated circuit pin grid array containing the 64 comparators (SPEC).

III technology. Each PGA has 64 comparators in a parallel array, a flip-flop (latch) at the output of each comparator, and a digital encoder that translates the thermometer code into a binary representation. A schematic diagram of the PGA is shown in Fig. 9. The system clock (offset differential ECL) derived from the detected laser pulse is used to register the comparator outputs. The layout of the clock distribution network within the GaAs circuit is shown in Fig. 10. The reference inputs are used to supply the individual comparators with a matching threshold voltage. To prevent the distortion and tuning problems characteristic of resistive ladders, each matching threshold voltage is supplied with a 13-bit digital-to-analog converter (Maxim MAX457). A 13-bit accuracy is required due to the non-linear spacing between threshold levels.



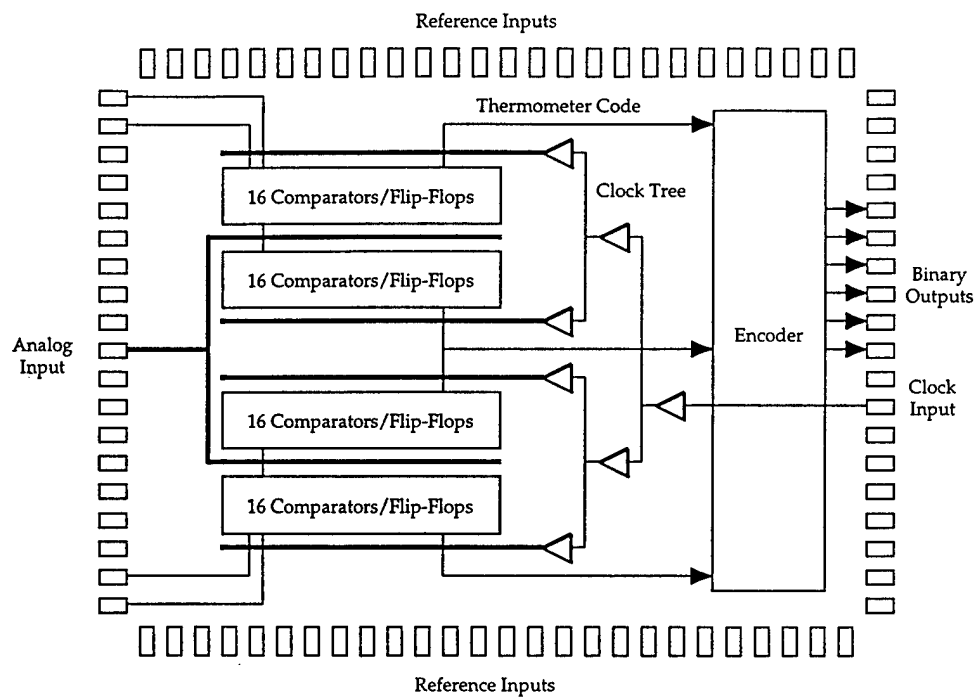


Figure 10: Clock distribution within the GaAs integrated circuit pin grid array (SPEC).

A single comparator layout is shown in Fig. 11 with the complete array layout shown in Fig. 12. To determine the response of the comparator array SPEC performed a SPICE simulation on a network that closely models the comparator parameters. The printed circuit board terminator, packaging, and wirebond were modeled as shown in Fig. 13. SPICE simulations of the network for the following process and temperature corners were performed:

Process	Temperature
Typical Process	25°
Slow Process	0°
Fast Process	85°

The results of the simulation are shown in Figs. 14 through 16, respectively. In each case, the comparator circuit compared the magnitude of a pulse to a 3 volt reference input. Two pulse magnitudes were evaluated (2.9995 V and 3.0005 V). The output of the comparator circuit was observed to determine if a correct output response would be produced (logic low and logic high, respectively). As shown, a correct response was obtained over the three process and temperature corners. The SPICE simulations and analysis of comparator circuits led to the following conclusions by SPEC:

1. The comparator circuit requires approximately 2 ns to obtain a correct output level from the onset of the pulse.
2. The SPICE analysis indicates that the comparator circuit can correctly sense  $\pm 0.5$  mV offsets relative to the 3 V reference. This has been determined to be the limit of sensitivity for the comparator circuit. This limit is set by the gain of the GaAs MESFETs used in the comparator circuit. Adding additional gain

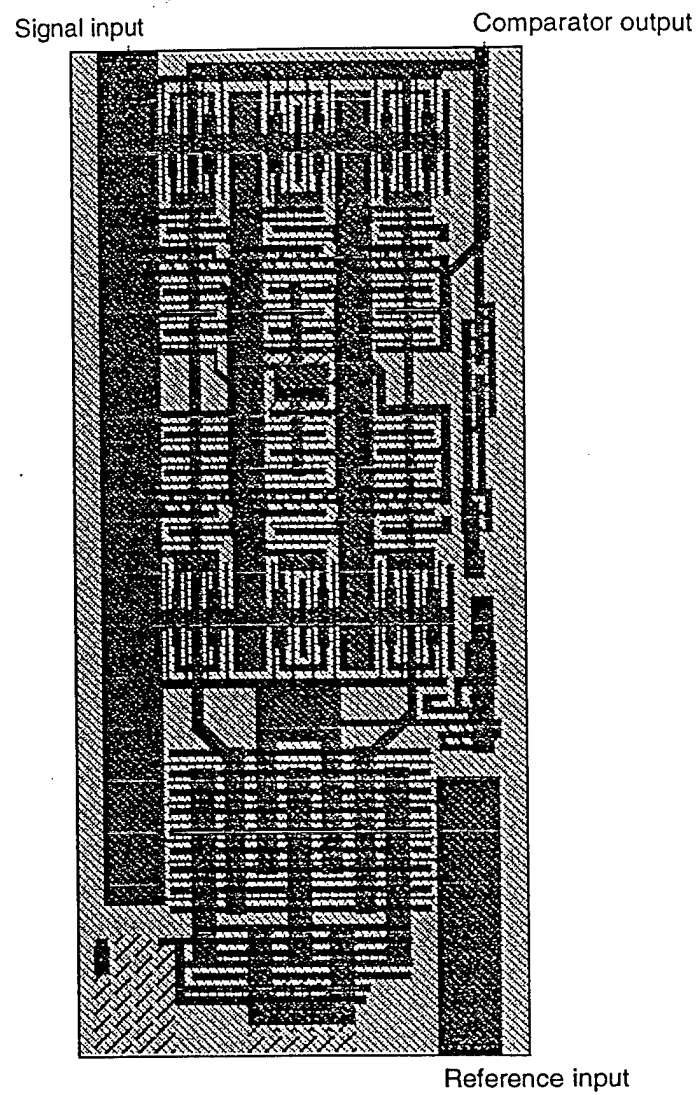


Figure 11: GaAs comparator layout (SPEC).

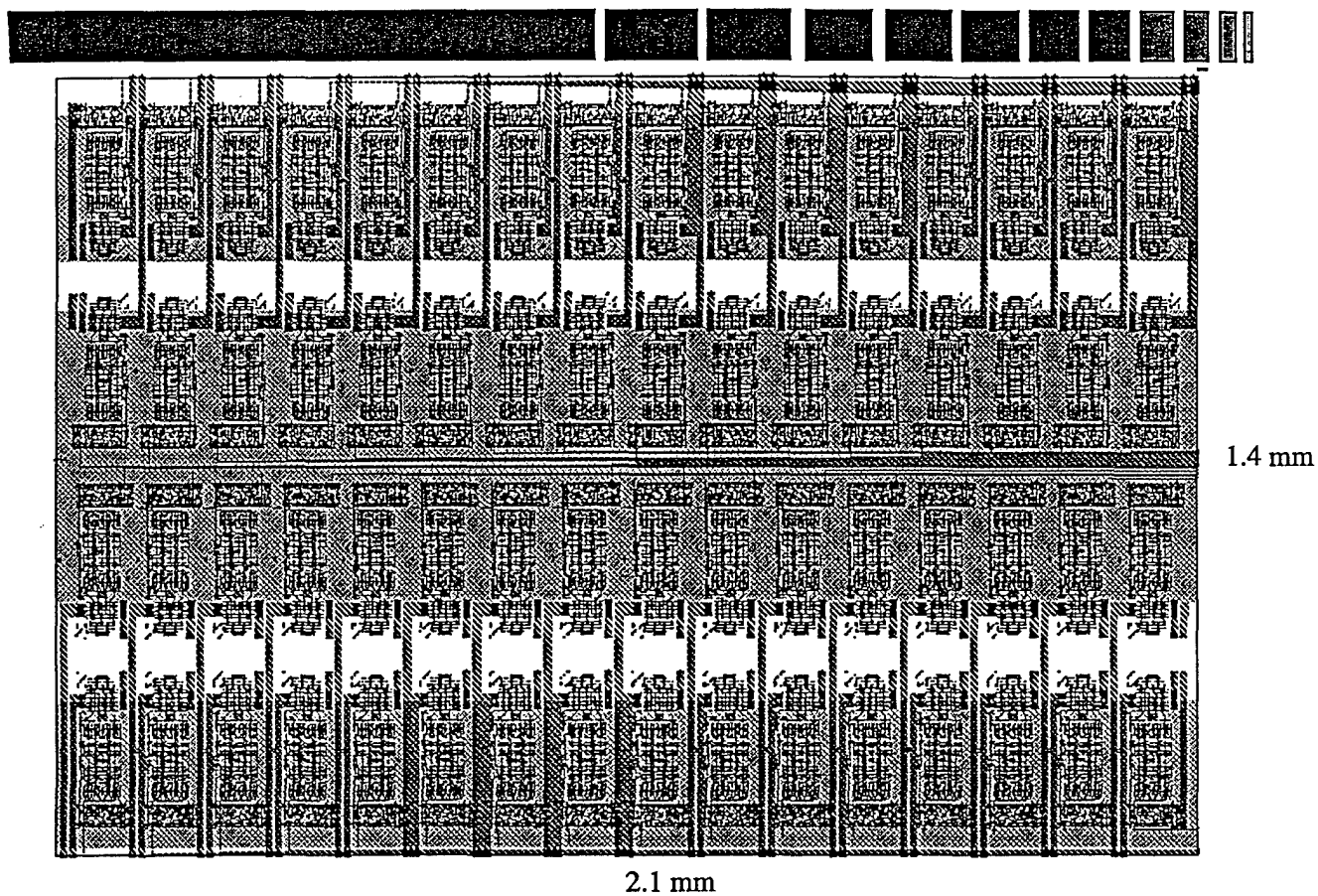


Figure 12: Comparator array layout 64 comparators (SPEC).

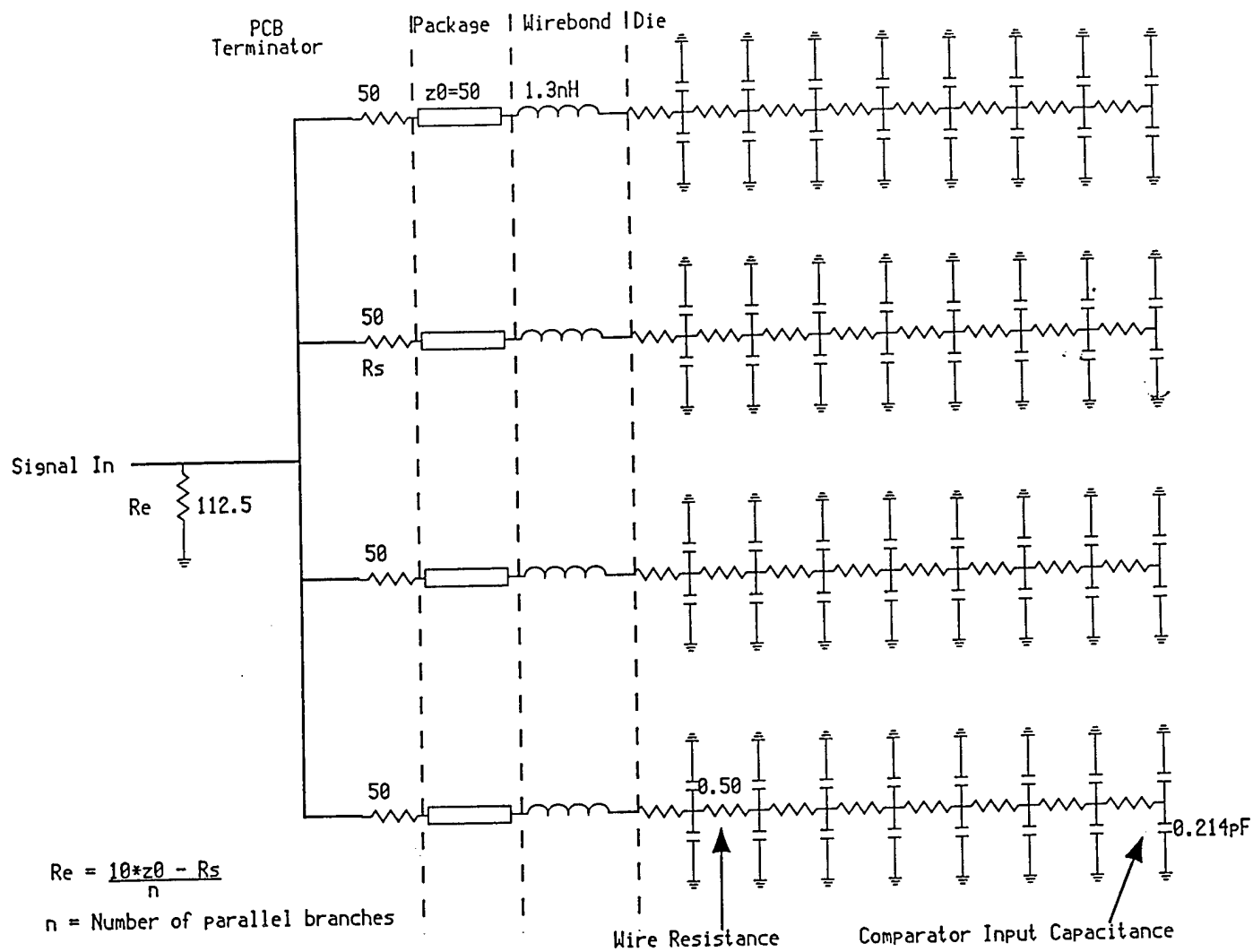


Figure 13: Schematic diagram for the SPICE simulation of the comparators (SPEC).

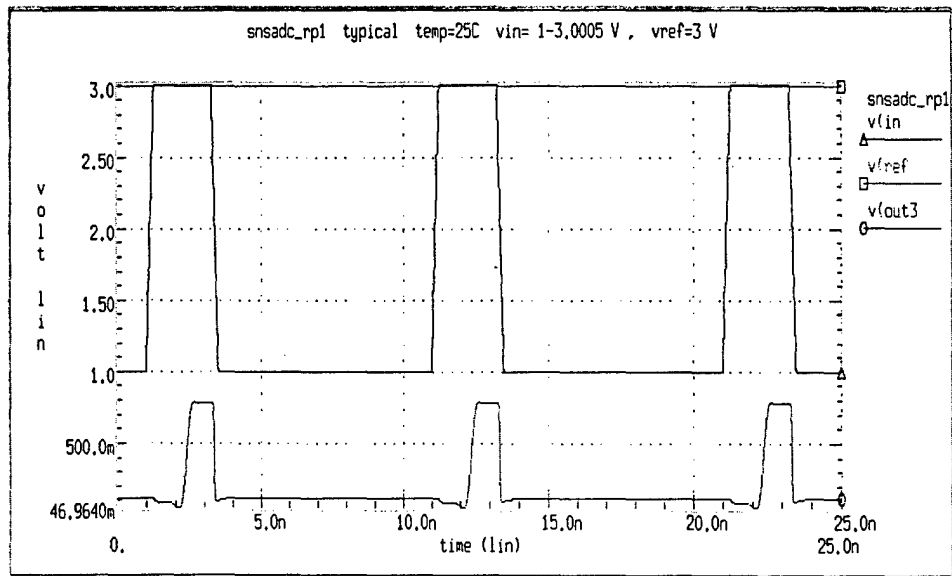
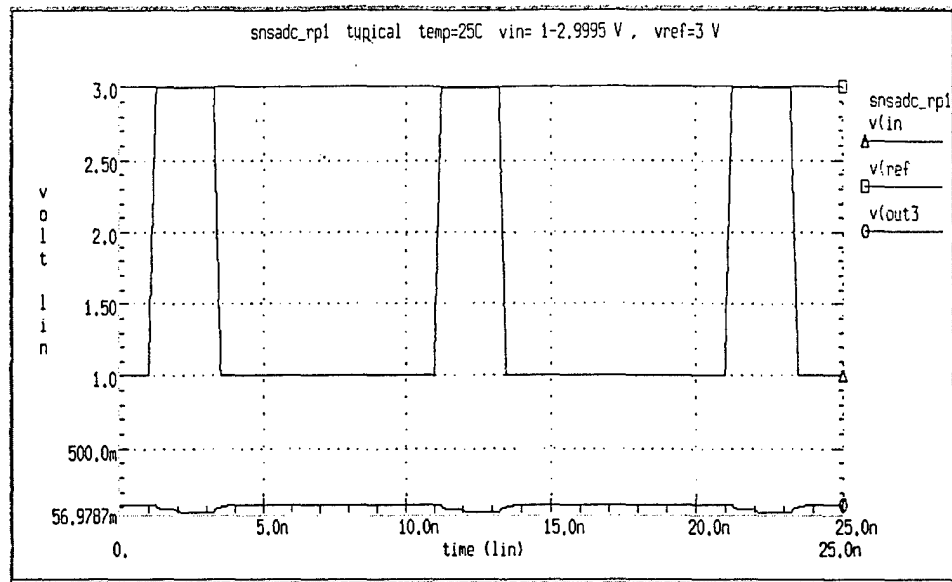


Figure 14: SPICE simulation results for the comparator array (Process = typical,  $T = 25^{\circ}\text{C}$ ) a)  $V_t = 2.0\text{ V}$ ,  $V_{in} = 2.9995\text{ V}$ , and b)  $V_t = 3.0\text{ V}$ ,  $V_{in} = 3.0005\text{ V}$  (SPEC).

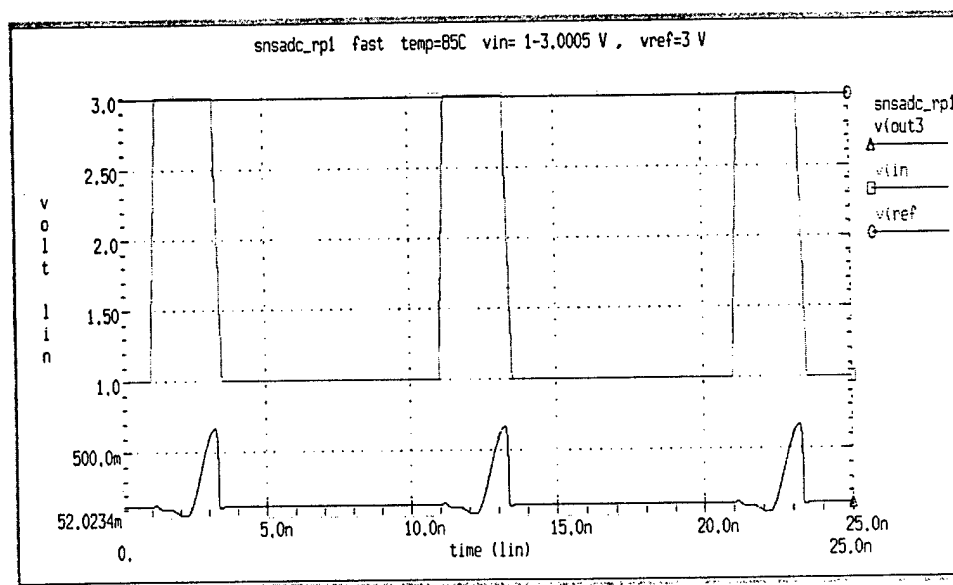
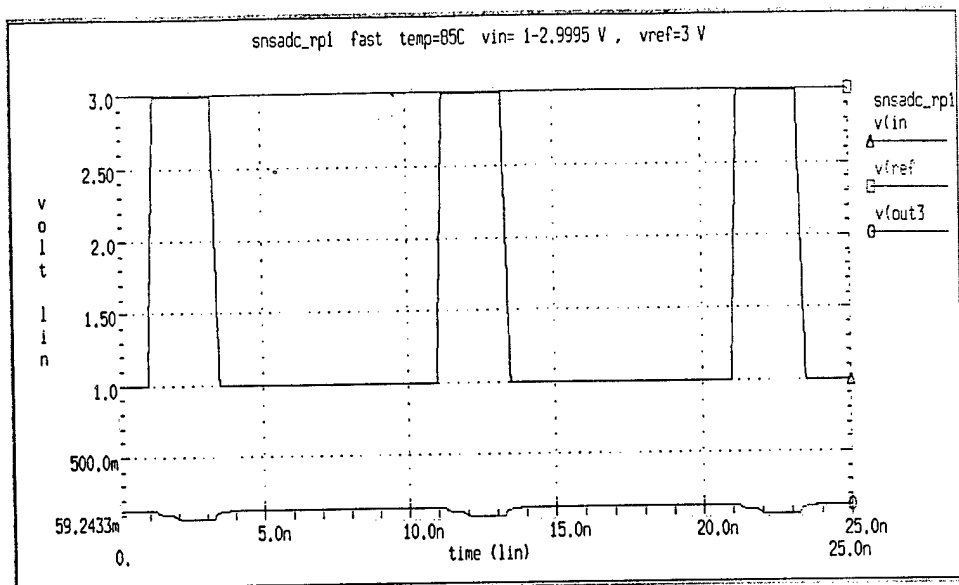


Figure 15: SPICE simulation results for the comparator array (Process = fast,  $T = 85^{\circ}\text{C}$ ) a)  $V_t = 3.0\text{ V}$ ,  $V_{in} = 2.9995\text{ V}$ , and b)  $V_t = 3.0\text{ V}$ ,  $V_{in} = 3.0005\text{ V}$  (SPEC).

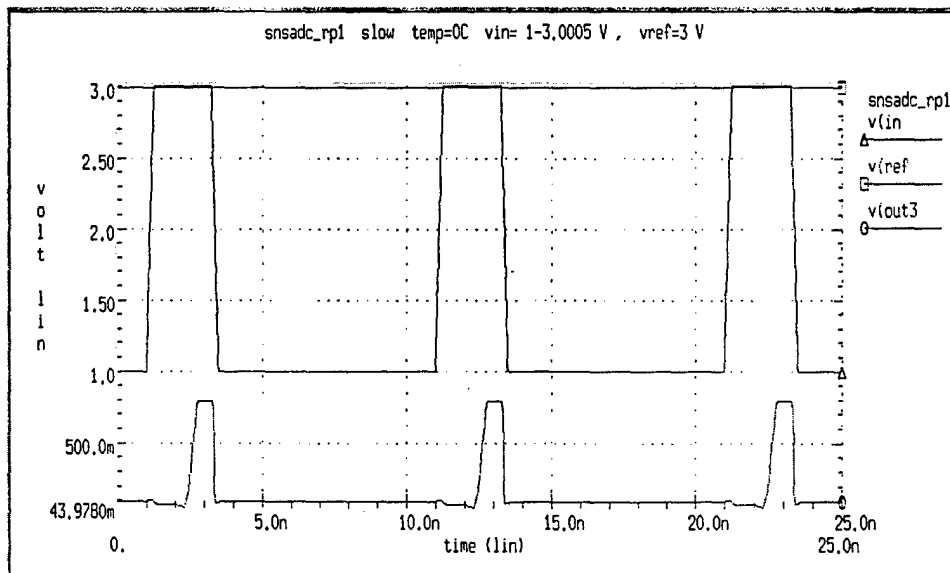
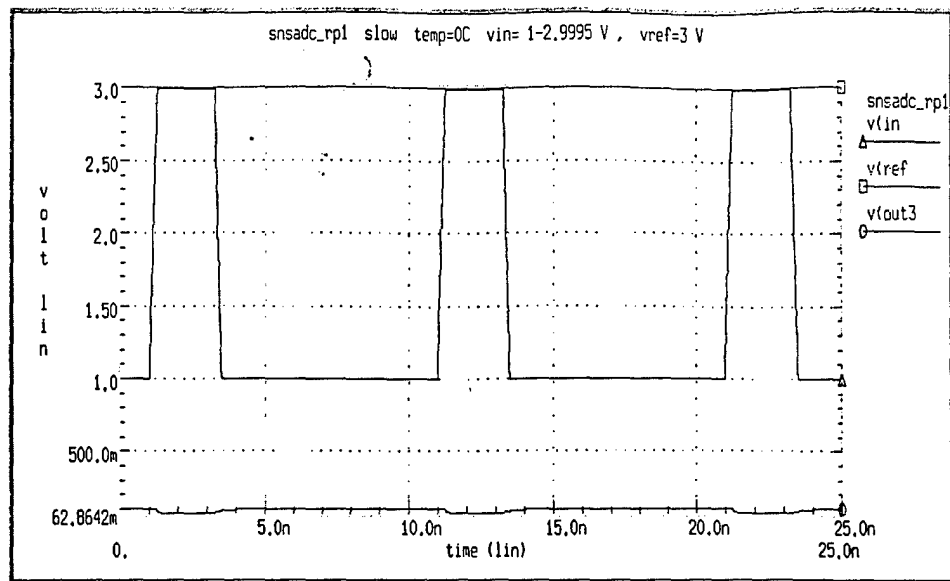


Figure 16: SPICE simulation results for the comparator array (Process = slow,  $T = 0^\circ$  C) a)  $V_t = 3.0$  V,  $V_{in} = 2.9995$  V, and b)  $V_t = 3.0$  V,  $V_{in} = 3.0005$  V (SPEC).

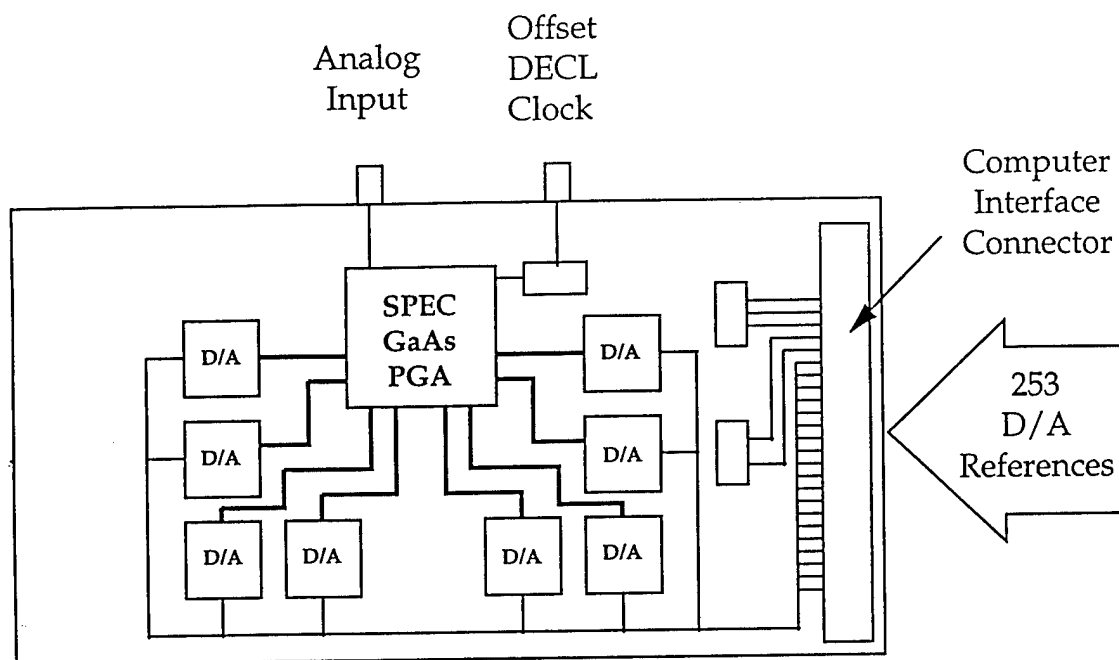


stages to increase comparator sensitivity will require additional setting time, i.e., a wider pulse.

3. In addition, the SPICE simulation does not show transistor threshold variations which occur in Vitesse's process. Vitesse has indicated that slight differences in processed transistor sizes can lead to offsets of up to 10 mV in adjacent transistors. In theory, these offsets can be calibrated out by adjusting the reference voltage.

One digital board is required for both the  $m_2$  and  $m_3$  channel. The minimum modulus ( $m_1$ ) requires two digital boards. A block diagram of the digital board (one of four) is shown in Fig. 17 and shows the position of the PGA integrated circuit and the eight DACs. The control words for each octal DAC (eight DACs per chip) are generated using a virtual instrument within LabView. Also shown are the connectors for the analog input and the offset differential emitter coupled logic (DECL) clock.

The 28 bits ( $7 \times 4$ ) coming from the digital boards are used to resolve the amplitude of the incoming signal. Figure 18 shows the programmable logic array (logic block) used to convert the SNS representation of the input signal into a more convenient binary code. The parity circuit uses the 14 bits from the minimum modulus channel (two digital boards) to determine whether a sample lies within the small band centered about each code transition point. If the sample lies within a code transition band, the parity is *even*. Otherwise, the parity is *odd*. The parity and the 14-bit word (from the PLA) are clocked in parallel through a 5-state buffer. The buffer allows the 14-bit word to be replaced with an interpolated value depending on the value of the parity. If the parity is odd (good sample), the 14-bit word is clocked through the buffer unaltered. If the parity is even, the values ahead and behind the even parity



4 of these  
(1 for each channel)

Figure 17: Block diagram of the digital processor containing eight octal DACs to control the threshold voltages on the GaAs pin grid array.

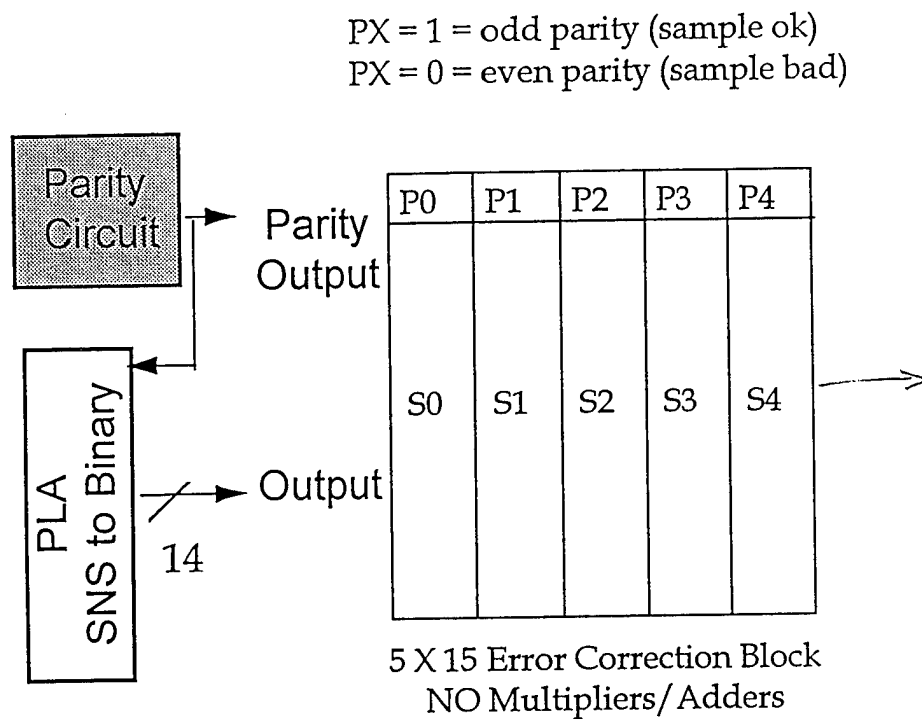


Figure 18: Interpolation architecture containing a 5 state buffer, a parity circuit (minimum modulus), and the logic block for SNS to binary conversion.

value are used to interpolate the possible encoding error. The interpolation process compares the most significant bits (MSBs) of the odd parity words stopping at the point where the MSBs do not agree. The MSBs that are the same are copied into the MSBs for the even parity word. The LSBs come directly from the original (even parity) word. Figure 19 shows an example where there is one out of five possible bad samples. In the interpolation process, P2 and P0 combine to form the MSBs of T1 (an intermediate state). The LSBs of T1 come from P1. At time  $t + 1$ , T1 is shifted into P2. The situation where two samples are even parity is shown in Fig. 20. In this case P3 and P0 combine to form the MSBs of T1 and T2. The LSBs of T1 and T2 are copied directly from P1 and P2. T1 is shifted into P2 and T2 is shifted into P3 at  $t + 1$ . The interpolation procedure for three out of five samples having even parity is shown in Fig. 21. The interpolation procedure for four out of five samples having even parity is shown in Fig. 22.

The 14-bit 5 MHz ADC is currently being constructed and will be tested in September 1996. The test setup to be used is shown in Fig. 23. A binary signal generator is used to supply the digital codes to a 16-bit digital-to-analog converter (DAC) to supply the test signal. The test signal is amplified using a power amplifier followed by a low-pass anti-aliasing filter. The 14-bit digital code at the SNS ADC output is examined using a logic analyzer that is connected to the computer controlling the test procedure. The computer also supplies the 253 DAC threshold voltages to the PGAs (using LabView). These tests and test results will be reported at a later date.



2/5 bad samples											
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					T1	T2	P0	P1	P2	P3	P4
					1	1	x	1	1	1	1
					-	-	-	-	-	-	-
MSB	1	1	0	1	1	1	1	X	1	1	1
	1	0	0	1	1	1	1	X	1	1	1
	1	0	0	1	1	1	1	X	1	1	1
	1	1	0	1	1	1	1	X	1	1	1
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	0	0	0	1	1	0	0	X	0	0	1
	0	1	0	0	0	1	0	X	0	1	0
	0	1	0	0	0	1	0	X	0	1	0
	1	1	1	1	1	1	1	X	1	1	1
	0	1	0	0	1	1	0	X	0	1	0
	0	1	0	0	0	1	0	X	0	1	0
	1	1	1	1	1	1	1	X	1	1	1
LSB	1	1	1	1	1	1	1	X	1	1	1

t

t+1

P3 and P0 combine to form MSBs of T1 and T2. LSBs of T1 and T2 are copied directly from P1 and P2. T1 is shifted into P2 rather than P1. T2 is shifted into P3.

P3 and P0 combine to form MSBs of T1 and T2. LSBs of T1 and T2 are copied directly from P1 and P2. T1 is shifted into P2 rather than P1. T2 is shifted into P3.

Figure 20: Interpolation processing with two out of five samples having even parity.



4/5 bad samples											
	P0	P1	P2	P3	P4		P0	P1	P2	P3	P4
	0	0	0	0	1		X	0	0	0	1
	-	-	-	-	-		-	-	-	-	-
MSB	1	1	0	1	1		X	1	0	0	1
	1	0	0	0	1		X	1	0	0	1
	1	0	0	0	1		X	1	0	0	1
	1	1	0	1	1		X	1	0	0	1
	0	0	0	0	0		X	0	0	0	0
	1	0	0	0	0		X	1	0	0	0
	0	0	0	1	1		X	0	0	0	1
	0	1	0	0	0		X	0	0	0	0
	0	1	0	0	0		X	0	0	0	0
	1	1	1	1	1		X	1	1	1	1
	0	1	0	0	0		X	0	0	0	0
	0	1	0	0	0		X	0	0	0	0
	1	1	1	1	0		X	1	1	1	0
LSB	1	1	1	1	0		X	1	1	1	0
	t						t+1				

P4 is retained.  
P3 is discarded.

Figure 22: Interpolation processing with four out of five samples having even parity.



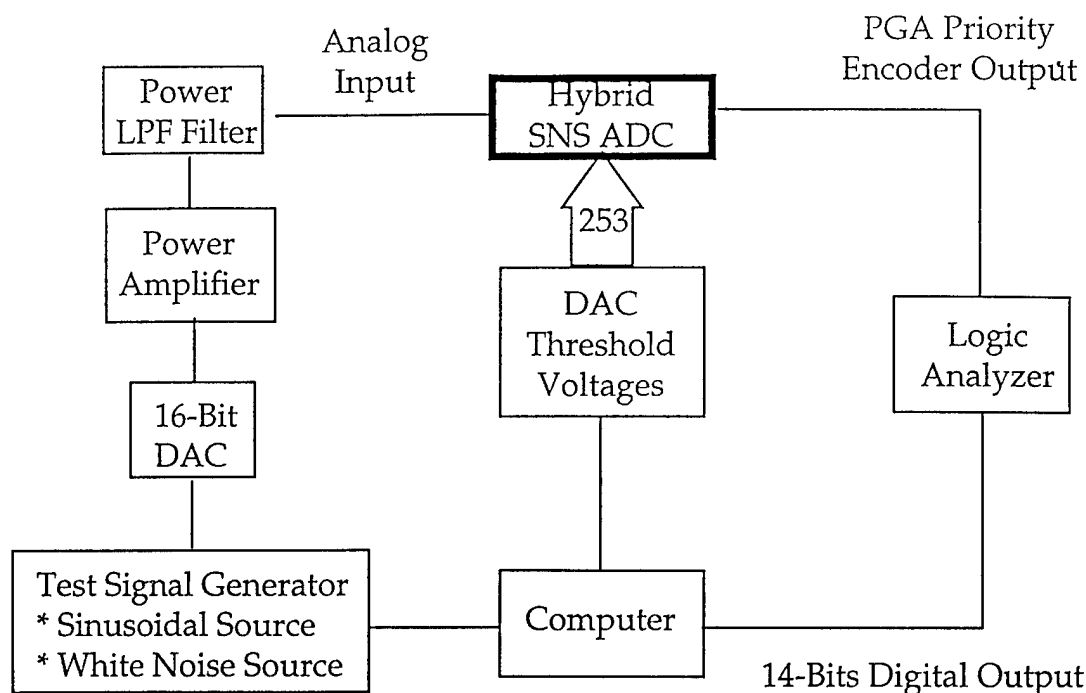


Figure 23: Block diagram of the laboratory setup for static and dynamic testing of the SNS ADC.

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